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# An Overview of a PC Based Data Acquisition System

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**Abstract**

This article starts briefly describing conventional A/D conversion. It proceeds to examine the architecture of data acquisition systems. We subsequently describe a data acquisition system which has been designed and implemented at DSP Laboratory, Department of Computer Science and Engineering, "Politehnica" University of Timişoara.

## 1 Introduction

Signal processing is a technique that we can use to gather data from the real world and make sense of it. Our brain works as a kind of signal processor. Every day, our senses collect external stimuli and send the information to our brain, where it is interpreted and used to trigger an appropriate response. For some time, engineers have adapted this idea to develop electronic systems able to extract and process real world signals and turn them into useful data. Initially this development was done using analog technology but, since the rapid advancement of the semiconductor industry during the 1980s, engineers have turned to digital signal processing as a more flexible and convenient method. Data acquisition in the general sense is the process of collecting information from the real world. For most engineers and scientists this data is mostly numerical and is usually collected, stored, and analyzed using a computer. The use of a computer automates the data acquisition process, enabling the collection of more data in less time with fewer errors.

## 1.1 Conventional A/D Conversion

### 1.1.1 Sampling and Analog-to-Digital Conversion

Sampling or conversion rate is the analog-to-digital conversion (ADC) specification most often examined. In the sampling process, a continuous time signal is sampled at uniformly spaced time intervals, $T_s$. The samples, $x[n]$, of the continuous time signal, $x(t)$ can be represented as $x[n] = x(nT_s)$. The effect, in the frequency domain, of the sampling process is to create periodically repeated versions of the signal spectrum at multiples of the sampling frequency $fs = 1/Ts$[Aziz]. This relationship is written in Eq. 1, where $X_s(t)$ represents the spectrum of the sampled signal, and $X(f)$ is the spectrum of the original continuous time signal.

$$x_s(f) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} X(f - kf_s) \tag{1}$$

The case where $f_s = 2f_B$ is known as Nyquist rate sampling, and $f_B$ is the bandwidth of the signal. Put another way, only signals whose highest frequency components are no more than one-half the sampling frequency can be accurately digitized. This rule is called the Nyquist theorem. Interference between repeated versions of the signal spectrum is known as aliasing and it prevents reconstruction of the signal. Multitudes of techniques are used to produce an analog-to-digital converter. Qualitative bandwidth and resolution tradeoffs of some at these A/D techniques are shown in Figure 1. As it is evident from Figure 1, sigma-delta A/D converters attain the highest resolution for relatively low signal bandwidths, and flash converters attain the highest bandwidths for relatively low resolution.

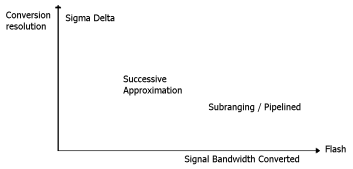


Figure 1. Bandwidth resolution tradeoffs

### 1.1.2 Dynamic Range

The concept of dynamic range is very important for data acquisition systems. By definition, the dynamic range of a data acquisition system is the ratio of the maximum value that can be measured to the smallest value that can be resolved [Austerlitz, pp.40–50]. This number is often represented in decibels (dB) as

$$Dynamic\ range\ (dB) = 20 \log \frac{u_{imax}}{u_{imin}} \tag{2}$$

For example, a data acquisition system with a 1-millivolt resolution and a value range of 0 to 10 volts (or -5 to +5 volts) has a dynamic range of 10000:1, or 80 dB. This dynamic range requires a minimum of 14 bits to represent it, since $2^{14} = 16384$, which is greater than 10000, while $2^{13} = 8192$ is less than 10000. The reverse process of converting digital data to an analog signal is called digital-to-analog conversion, and the device that does this is called a digital-to-analog converter (DACs). Some common applications for DACs include control systems, waveform generators, and speech synthesisers.

## 1.2 Data Acquisition System Architecture

According to [Toma and Burr-Brown] there are several different types of data acquisition system architecture, depending on where the analogue multiplexer is connected.

1. Data acquisition system with multiplexing of the analogue input signals.
2. Data acquisition system with multiplexing of the outputs of S/H circuits.
3. Data acquisition system with multiplexing of the outputs of ADC.

In this article has been described only the first type of architecture. The data acquisition system with multiplexing of analogue input signals is the most commonly used architecture. From the point of view of cost, it is the cheapest architecture, but at the same time, it doesn't achieve the highest speed of data acquisition. Furthermore, the ADC samples one channel, switches to the next channel, samples it, switches to the next channel, and so on. Because the same ADC is sampling many channels instead of one, the effective rate of each individual channel is inversely proportional to the number of channels sampled. As an example, an ADC sampling at 100 kS/s on 10 channels will effectively sample each individual channel at:

$$\frac{100kS/s}{10channels} = 10kS/s\,per\,channel \tag{3}$$

A data acquisition system with multiplexing of analogue signals is shown in Figure 2.

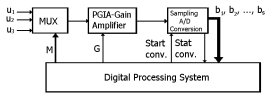


Figure 2. Data acquisition system with multiplexing of analogue signals

The major functions are described in the following paragraphs.

**A multiplexer (MUX)** allows a single amplifier, S/H and ADC to be 'time-shared' over several analogue channels, thus saving on costs [Cook].

**An instrumentation amplifier** is a differential-mode amplifier with the desirable characteristics of precise $A_{DM}$, low-signal input currents, and the ability to supply sufficient output current to a load. An instrumentation amplifier allows the dynamic range of the input analogue signal to be increased.

**A sample/hold (S/H) circuit** is used to overcome a problem that can arise with an ADC. In many types of ADC, such as successive approximations, a change in the input voltage during the conversion process can result in an erroneous digital output.To achieve a conversion uncertainty of less than $\pm\frac{1}{2}LSB$, then the voltage must change by less than this amount over the time it takes to do a conversion, $t_{con}$.

**A/D Conversion** has been described above.

**A digital processing system** is usually used to implement all command and control functions of the data acquisition process. A digital processing system can be implemented using controller (like 8051), microprocessor, or a PC. In our case, an IBM PC computer has been used. Note that a data acquisition system is usually a plug-in board.

# 2 Data acquisition system AQUARIUS — DSP 1 for the IBM PC

## 2.1 Introduction

The architecture of a system which executes data acquisition using multiplexing of input channels was used as a prototype of the data acquisition system which has been implemented. We introduced the kind

of the system outlined above. This type of architecture was improved by adding the techniques of real-time data acquisition using interrupts and direct memory access. These techniques produce considerably reductions in the time needed for data acquisition. At the same time, data acquisition by interrupts at speeds close to 100kS/s can lead to the loss of samples. This problem can be avoided by using FIFO memory placed at the output of the ADC. The next generation of this system will have an on-board FIFO memory.

### 2.1.1 Features

- Fast, 12-bit ADC
  - 100 kS/s sustained sampling rate;
  - 8 single-ended or 8 differential channels;
  - Hardware -selectable range: 0 to 20 V, (+10 V, -10V), or 0 to 10V, (+5 V, -5V);
- 1 Resistor Ladder Network, buffered, 12-bit DAC
  - Hardware -selectable range: 0 to 20 V, (+10 V, -10V), or 0 to 10 V, (+5V, -5V)
- 3 independent 16-bit counters/timers
- Three 8-bit ports with handshaking and interrupt capabilities
- 16-bit DMA

## 2.2 Hardware

**Analogue Input** – Firstly, the Aquarius-DSP 1 uses CMOS analogue input multiplexer MPC507A connected to analogue input channels. The multiplexer has input overvoltage protection of (70 V) powered on. Analogue input channels can be used as 8 single-ended inputs, or 8 fully differential inputs (software selectable). Voltage input ranges are hardware selectable for 0 to 20 V, or (+10 V, -10V), 0 to 10 V, or (+5

V, -5V).
Secondly, it has a 12-bit sampling ADC Burr-Brown ADS774 that gives an analogue resolution of 2.44 mV with an input range of 10V, or 9.8 mV with an input range of 20V.
Thirdly, the data acquisition system performs both single A/D conversions and multiple A/D conversions of a fixed number of samples. Multiple A/D conversions can be handled by programmed I/O, interrupts, or DMA.
Finally, the Aquarius-DSP 1 acquires data in two modes:
1) continuous acquisition of a single channel, 2) multichannel acquisition with continuous scanning.

**Analogue Output** – The Aquarius-DSP 1 has a buffered, resistor ladder network, 12-bit DAC80 connected to an analogue output channel. The output channel can be configured for unipolar (0 to 10 V, 0 to 20V) or bipolar (+5V, -5V, or +10V, -10V) operation.

**Digital I/O** – Digital I/O interfaces are often used on PC DAQ systems to control processes, generate patterns for testing, and communicate with peripheral equipment. The Aquarius-DSP 1 provides 24 digital I/O lines through the i8255 PPI chip. The 8255 consists of three 8-bit ports, PA, PB, and PC, which can be programmed as either inputs or outputs. Ports PA and PB are always used for digital I/O, while port PC can be configured for either data I/O or control, status, and handshake signals.

**Counter/Timer** – Counter/timer circuitry is useful for many applications, including counting the occurrences of a digital event, digital pulse timing, and generating square waves and pulses. The Aquarius-DSP 1 uses the i8253/8254 counter/timer for time-related functions. The i8253 has three independent 16-bit counters/timers, which can be individually configured. Counter 0 is reserved for multiple A/D conversion timing. Counter 1 is reserved for DMA mode. Counter 2 is reserved for multiple D/A conversion timing.

**PC AT I/O Channel Interface** – The PC AT I/O channel interface circuitry includes address latches, address decoding circuitry, data buffers, and interface timing and control signals. Interrupt lines 5, 10, 11, or 15 are available on the board. Full use can be made of AT bus 16-bit DMA transfers on DMA channels 5, 6, or 7.

## 3 Conclusions

The data acquisition system described above has been successfully implemented. The tests we made show that data can be acquired at speeds close to 100 kS/s. Also, we tested the functioning of the data acquisition system by test programs and data acquisition drivers. We achieved accuracy levels close to these of ADC.

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## References

[1] Pervez M. Aziz, Henrik V. Sorensen and Jan Van Spiegel. An Overview of Sigma-Delta Converters, IEEE Signal Processing Magazine, January, 1996, pp.61–84.

[2] Howard Austerlitz. Data Acquisition Techniques Using Personal Computers, San Diego, 1991, pp.40–50.

[3] *** The Handbook of Personal Computer for Data Acquisition, Test, Measurment and Control, Burr-Brown, 4th Edition, 1989.

[4] Liviu Toma. Sisteme de Achizitie si Prelucrare Numerica a Semnalelor, Editura de Vest, Timisoara, 1996, pp.86–108.

[5] Barry M. Cook, Neil H. White. Computer Peripherals, Edward Arnold, 1995, pp.185–198.

[6] Mihai Micea, Iurie Guzun, and Viaceslav Guzun. Performant Multifunction I/O Board for the IBM PC AT, in Proc. Int. Conf. On Microelectronics and Computer Sciemce (ICMCS), vol. 1, (Chisinau, Moldova), pp.167–171 October, 1997.

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